IN THE CLAIMS

1. (Previously Presented) A memory cell, comprising:

a pair of cross coupled inverters, wherein each inverter includes an NMOS transistor and a PMOS transistor, and wherein at least one of the NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3), wherein the low tunnel barrier intergate insulator includes a further transition metal oxide; and

a pair of bitlines coupled to the pair of cross inverters at a pair of voltage nodes.

2. (Original) The memory cell of claim 1, wherein the floating gate is adapted to be programmed with a charge such that the memory cell has a definitive asymmetry and a definitive state upon startup.

3-4. (Canceled)

5. (Previously Presented) The memory cell of claim 1, wherein the further transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

6. (Original) The memory cell of claim 1, wherein the low tunnel barrier intergate insulator includes a Perovskite oxide tunnel barrier.

7. (Previously Presented) A memory cell, comprising:

a pair of cross coupled inverters, wherein each inverter includes an NMOS transistor and a PMOS transistor, and wherein at least one of the NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator; and

a pair of bitlines coupled to the pair of cross inverters at a pair of voltage nodes.

8. (Previously Presented) A memory cell, comprising:

a pair of cross coupled inverters, wherein each inverter includes an NMOS transistor and a PMOS transistor, and wherein at least one of the NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator; and

a pair of bitlines coupled to the pair of cross inverters at a pair of voltage nodes.

9. (Previously Presented) A four transistor SRAM cell, comprising:

a pair of cross coupled NMOS floating gate transistors, wherein each of the pair of cross coupled NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

a pair of bitlines coupled to the pair of cross coupled NMOS floating gate transistors at a pair of voltage nodes through a pair of access transistors;

wherein the floating gates are adapted to be programmed with a respective charge state such that the SRAM cell has a definitive asymmetry;

wherein the low tunnel barrier intergate insulator includes a metal layer in contact with one of the floating gate and the control gate.

10. (Original) The memory cell of claim 9, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

11. (Previously Presented) A four transistor SRAM cell, comprising:

a pair of cross coupled NMOS floating gate transistors, wherein each of the pair of cross coupled NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

a pair of bitlines coupled to the pair of cross coupled NMOS floating gate transistors at a pair of voltage nodes through a pair of access transistors;

wherein the floating gates are adapted to be programmed with a respective charge state such that the SRAM cell has a definitive asymmetry; and

wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

12. (Original) The memory cell of claim 11, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

13-18. (Canceled)

19. (Currently Amended) A memory array, comprising:

a number of memory cells, wherein each memory cell includes:

a pair of cross coupled inverters, wherein each inverter includes an NMOS transistor and a PMOS transistor, and wherein at least one of the NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

wherein the low tunnel barrier ~~integrate~~ intergate insulator includes a metal layer in contact with one of the floating gate and the control gate;

a pair of bitlines coupled to the pair of cross inverters at a pair of voltage nodes through a pair of access transistors; and

a wordline coupled to the pair of access transistors.

20. (Original) The memory array of claim 19, wherein the floating gate is adapted to be programmed with a charge such that the memory cell has a definitive asymmetry and a definitive state upon startup.

21. (Original) The memory array of claim 19, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

22. (Previously Presented) A memory array, comprising:

a number of memory cells, wherein each memory cell includes:

a pair of cross coupled inverters, wherein each inverter includes an NMOS transistor and a PMOS transistor, and wherein at least one of the NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator; and

wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator;

a pair of bitlines coupled to the pair of cross inverters at a pair of voltage nodes through a pair of access transistors; and

a wordline coupled to the pair of access transistors.

23. (Previously Presented) A memory array, comprising:

a number of memory cells, wherein each memory cell includes:

a pair of cross coupled inverters, wherein each inverter includes an NMOS transistor and a PMOS transistor, and wherein at least one of the NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator; and

wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator;

a pair of bitlines coupled to the pair of cross inverters at a pair of voltage nodes through a pair of access transistors; and

a wordline coupled to the pair of access transistors..

24. (Currently Amended) An array of four transistor SRAM cells, comprising:

a pair of cross coupled NMOS floating gate transistors, wherein each of the pair of cross coupled NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

wherein the low tunnel barrier ~~integrate~~ intergate insulator includes a metal layer in contact with one of the floating gate and the control gate;

a pair of bitlines coupled to the pair of cross coupled NMOS floating gate transistors at a pair of voltage nodes through a pair of access transistors;

a wordline coupled to the pair of access transistors; and

wherein the floating gates are adapted to be programmed with a respective charge state such that the SRAM cell has a definitive asymmetry.

25. (Original) The array of memory cells of claim 24, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

26. (Previously Presented) An array of memory cells, comprising:

a pair of cross coupled NMOS floating gate transistors, wherein each of the pair of cross coupled NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

wherein each floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator;

a pair of bitlines coupled to the pair of cross coupled NMOS floating gate transistors at a pair of voltage nodes through a pair of access transistors;

a wordline coupled to the pair of access transistors; and

wherein the floating gates are adapted to be programmed with a respective charge state such that the SRAM cell has a definitive asymmetry.

27. (Previously Presented) An array of memory cells, comprising:

a pair of cross coupled NMOS floating gate transistors, wherein each of the pair of cross coupled NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator; and

wherein each control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator;

a pair of bitlines coupled to the pair of cross coupled NMOS floating gate transistors at a pair of voltage nodes through a pair of access transistors;

a wordline coupled to the pair of access transistors; and

wherein the floating gates are adapted to be programmed with a respective charge state such that the SRAM cell has a definitive asymmetry.

28. (Canceled)

29. (Currently Amended) An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes an array of memory cells, comprising:

a number of SRAM cells, wherein the number of SRAM cells each include a pair of cross coupled transistors, wherein at least one of the cross coupled transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

wherein the low tunnel barrier ~~integrate~~ intergate insulator includes a metal layer in contact with one of the floating gate and the control gate;

a pair of bitlines coupled to each SRAM cell and the pair of cross coupled transistors at a pair of voltage nodes through a pair of access transistors;

a wordline coupled to the pair of access transistors in each SRAM cell;

a sense amplifier coupled to the pairs of bitlines; and

wherein the floating gate is adapted to be programmed with a respective charge state such that each SRAM cell can have a definitive asymmetry.

30. (Original) The electronic system of claim 29, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

31. (Previously Presented) An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes an array of memory cells, comprising:

a number of SRAM cells, wherein the number of SRAM cells each include a pair of cross coupled transistors, wherein at least one of the cross coupled transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator; and

wherein each floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator;

a pair of bitlines coupled to each SRAM cell and the pair of cross coupled transistors at a pair of voltage nodes through a pair of access transistors;

a wordline coupled to the pair of access transistors in each SRAM cell;

a sense amplifier coupled to the pairs of bitlines; and

wherein the floating gate is adapted to be programmed with a respective charge state such that each SRAM cell can have a definitive asymmetry.

32. (Previously Presented) An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes an array of memory cells, comprising:

a number of SRAM cells, wherein the number of SRAM cells each include a pair of cross coupled transistors, wherein at least one of the cross coupled transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator; and

wherein each control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator;

a pair of bitlines coupled to each SRAM cell and the pair of cross coupled transistors at a pair of voltage nodes through a pair of access transistors;

a wordline coupled to the pair of access transistors in each SRAM cell;

a sense amplifier coupled to the pairs of bitlines; and

wherein the floating gate is adapted to be programmed with a respective charge state such that each SRAM cell can have a definitive asymmetry.

33. (Canceled)

34. (Previously Presented) The method of claim 37, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

35. (Previously Presented) The method of claim 37, wherein forming the low tunnel barrier intergate insulator includes forming a transition metal oxide insulator.

36. (Original) The method of claim 35, wherein forming the transition metal oxide insulator includes forming the transition metal oxide insulator selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

37. (Previously Presented) A method of forming a memory cell, comprising:

forming a pair of cross coupled inverters, wherein forming each inverter includes an NMOS transistor and a PMOS transistor, and wherein the method includes forming at least one of the NMOS transistors to include:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate

insulator such that the floating gate is adapted to be programmed with a charge and the memory cell can have a definitive asymmetry and a definitive state upon startup; and

forming a pair of bitlines coupled to the pair of cross inverters at a pair of voltage nodes; and

wherein forming the floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

38. (Previously Presented) A method of forming a memory cell, comprising:

forming a pair of cross coupled inverters, wherein forming each inverter includes an NMOS transistor and a PMOS transistor, and wherein the method includes forming at least one of the NMOS transistors to include:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator such that the floating gate is adapted to be programmed with a charge and the memory cell can have a definitive asymmetry and a definitive state upon startup; and

forming a pair of bitlines coupled to the pair of cross inverters at a pair of voltage nodes; and

wherein forming the control gate includes a forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

39. (Canceled)

40. (Previously Presented) The method of claim 41, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

41. (Previously Presented) A method for forming an array of memory cells, comprising:

forming at least one SRAM cell in the array, wherein forming the at least one SRAM cell includes forming a pair of cross coupled transistors, and wherein forming the pair of cross coupled transistors includes forming at least one of the cross coupled transistors to include:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator such that the floating gate is adapted to be programmed with a charge and the SRAM cell can have a definitive asymmetry and a definitive state upon startup;

forming a pair of bitlines coupled to the at least one SRAM cell and the pair of cross coupled transistors at a pair of voltage nodes through a pair of access transistors;

forming a wordline coupled to the pair of access transistors in the at least one SRAM cell; and

wherein forming each floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

42. (Previously Presented) A method for forming an array of memory cells, comprising:

forming at least one SRAM cell in the array, wherein forming the at least one SRAM cell includes forming a pair of cross coupled transistors, and wherein forming the pair of cross coupled transistors includes forming at least one of the cross coupled transistors to include:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator such that the floating gate is adapted to be programmed with a charge and the SRAM cell can have a definitive asymmetry and a definitive state upon startup;

forming a pair of bitlines coupled to the at least one SRAM cell and the pair of cross coupled transistors at a pair of voltage nodes through a pair of access transistors;

forming a wordline coupled to the pair of access transistors in the at least one SRAM cell; and

wherein forming each control gate includes forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

43. (Previously Presented) A method for operating an SRAM cell which includes a pair of cross coupled floating gate transistors, comprising:

writing to at least one of the cross coupled floating gates of the SRAM cell using channel hot electron injection, wherein the cross coupled floating gate transistors each include:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate;

sensing a logic state of the SRAM cell in a start up mode;

writing to the floating gate by tunneling electrons from the control gate to the floating gate .

44. (Original) The method of claim 43, wherein erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate further includes:

providing a negative voltage to the substrate of the at least one of the cross coupled floating gate transistors; and

providing a large positive voltage to the control gate of the at least one of the cross coupled floating gate transistors.

45. (Canceled)

46. (Previously Presented) The method of claim 43, wherein writing to the floating gate by tunneling electrons from the control gate to the floating gate further includes:

applying a positive voltage to the substrate of the at least one of the cross coupled transistors; and

applying a large negative voltage to the control gate of the at least one of the cross coupled transistors.

47. (Original) The method of claim 43, wherein erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate includes tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator.

48. (Original) The method of claim 47, wherein tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator includes tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

49. (Original) The method of claim 47, wherein tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator includes tunneling electrons from a metal layer formed on the floating gate in contact with the low tunnel barrier intergate insulator

to a metal layer formed on the control gate and also in contact with the low tunnel barrier intergate insulator.

50. (Previously Presented) A memory cell comprising:

a pair of cross coupled inverters, wherein each inverter includes an NMOS transistor and a POMS transistor, and wherein at least one of the NMOS transistors includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate, wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3);

a pair of bitlines coupled to the pair of cross inverters at a pair of voltage nodes; and wherein at least one of the control gate and the floating gate includes a polysilicon gate layer having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

Conclusion

Claims 19, 24, and 29 have been amended to correct spelling errors. It is respectfully submitted that these changes do not introduce new matter, and the claims are allowable without further search or consideration. Therefore, entry is appropriate under Rule 312, and is respectfully requested.

Respectfully submitted,

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